

Computing

Lesson 3: The FDE cycle

Computer systems

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Materials from the Teach Computing Curriculum created by the National Centre for Computing Education



Task 1 - Task name

Which component of the CPU is described in each line of this table?

Carries data around the CPU	
Regulates the cycles per second	
Instructs the other components	
Carries out mathematical operations	
Fast access memory locations in the CPU	



Fetch-decode-execute jumble

1	
2	
3	
4	
5	
6	
7	
8	
9	The cycle repeats

Fetch

Decode

Execute

The CPU executes the instruction

Instructions are loaded into RAM from secondary memory

The instruction is transferred via the data bus to the CPU

The result may be stored back into RAM

The CPU may fetch data held in memory if referenced in the instruction

The instructions are stored in RAM in numbered memory locations

The CPU sends a signal requesting an instruction from a specific location in RAM

The CPU decodes the instruction



The FDE cycle in action

Instruction

- Open oaknat.uk/comp-101comp-lmc
- Change the program using the dropdown menu in the bottom left hand corner, you want “Adding 2 inputs” (Hint on next slide)
- Run the program using the “Run Program” button. Watch the log as it runs

Question 1

What does **num1** represent on lines 2 & 4?

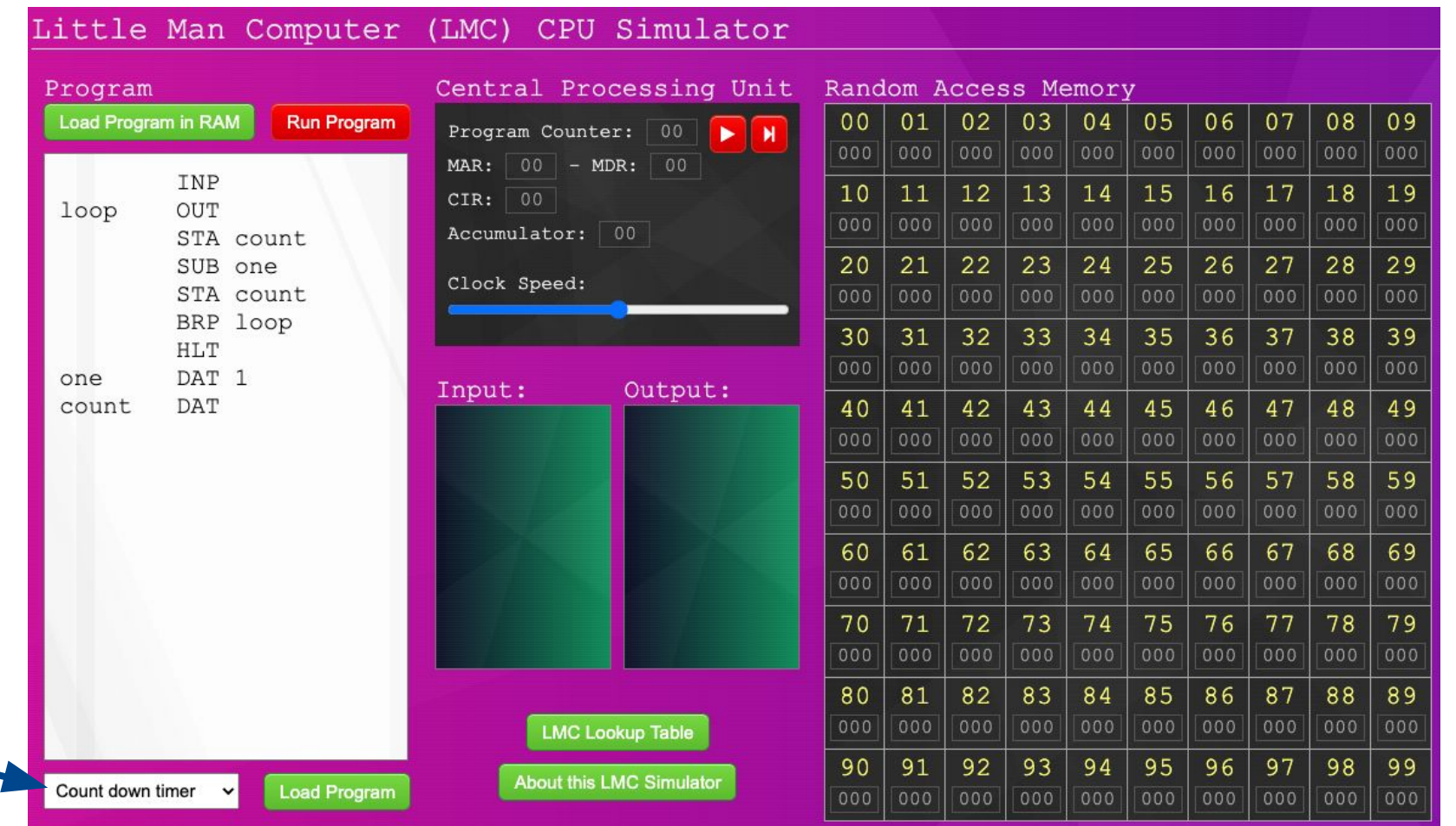
Question 2

What is the instruction number for **INP**?



The FDE cycle in action - Part 1

Change the program using the **dropdown menu** in the bottom left hand corner, you want “**Adding 2 inputs**”



Credit: Philippe Kerampran, 101computing



The FDE cycle in action - Part 2

Use the tables on the next 2 pages to note down what each component is doing during the cycle.

Little Man Computer (LMC) CPU Simulator

Program

Load Program in RAM

Run Program

loop

INP

OUT

STA count

SUB one

STA count

BRP loop

HLT

one

count

DAT 1

DAT

Central Processing Unit

Program Counter: 00

MAR: 00 - MDR: 00

CIR: 00

Accumulator: 00

Clock Speed:

Input:

Output:

LMC Lookup Table

About this LMC Simulator

Random Access Memory

00	01	02	03	04	05	06	07	08	09
000	000	000	000	000	000	000	000	000	000
10	11	12	13	14	15	16	17	18	19
000	000	000	000	000	000	000	000	000	000
20	21	22	23	24	25	26	27	28	29
000	000	000	000	000	000	000	000	000	000
30	31	32	33	34	35	36	37	38	39
000	000	000	000	000	000	000	000	000	000
40	41	42	43	44	45	46	47	48	49
000	000	000	000	000	000	000	000	000	000
50	51	52	53	54	55	56	57	58	59
000	000	000	000	000	000	000	000	000	000
60	61	62	63	64	65	66	67	68	69
000	000	000	000	000	000	000	000	000	000
70	71	72	73	74	75	76	77	78	79
000	000	000	000	000	000	000	000	000	000
80	81	82	83	84	85	86	87	88	89
000	000	000	000	000	000	000	000	000	000
90	91	92	93	94	95	96	97	98	99
000	000	000	000	000	000	000	000	000	000

Credit: Philippe Kerampran, 101computing



The FDE cycle in action

Component	Fetch	Decode	Execute
Control Unit			
ALU			
Buses			
Accumulator			



The FDE cycle in action

Component	Fetch	Decode	Execute
Memory address register			
Memory data register			
Current instruction register			
Program counter			

